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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/970,749	10/03/2001	Charles A. Miller	FORM 2209 (P139-US)	1647

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EXAMINER
DINH, TUAN T

ART UNIT	PAPER NUMBER
2827	

DATE MAILED: 11/19/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/970,749	MILLER, CHARLES A.	
	Examiner	Art Unit	
	Tuan T Dinh	2827	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 August 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-38* is/are pending in the application.

4a) Of the above claim(s) *1-20 and 32-38* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *21-31* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Response to Arguments

1. Applicant's arguments filed 8/26/02 have been fully considered but they are not persuasive.

Applicant argues:

(a) Hayashi fails to disclose the "base IC die", the "first secondary IC die", or the conductive contacts."

(b) Hayashi teaches "electronic elements but not teach they are ID die (page 2, lines 1-2)."

(d) Hayashi fails to teach "solder forms the first conductive signal paths."

(e) Hayashi fails to teach "the substrate is a semiconductor substrate."

(f) Hayashi fails to teach "second secondary IC die links by second conductive paths to the second surface of the base IC die."

Examiner disagrees.

Respond to arguments (a), (b) and (e), Hayashi shows in figure 1 a hybrid IC (1, column 4, line 43) having first and second surfaces. The first surface includes a plurality of electronic elements (3) and connection terminals (4) electrically connected to a printed circuit board (5, column 5, line 41). The printed circuit board (PCB-5) in general consider as a substrate , board substrate, or semiconductor substrate depending what terminology term or name to use. The hybrid IC (1) is consider as typed of a substrate or PCB having a body or a base to carry some electronic components. The electronic

components (3) typically is integrated circuit chips or IC chips which is consider as IC dies (for other terminology term); therefore, the hybrid IC body (1) can be considered as a base IC die (chip) having some IC chip or IC dies (3) on a surface of the base IC die (1). The connection terminal (4) is made by conductive material (metal or insulative material (column 4, lines 64-66) which are electrically connected between the base IC (1) and the substrate (5) by connection electrodes (2a)

Response to argument (d), Hayashi teaches connective contacts (4) are soldered to the connection electrodes (2a, column 4, lines 49-50). The connection electrodes are formed as pads of the base (1) for making electrical connection between the base IC die and the substrate. The routing connection of the pads (2a) can be formed as signal paths.

Response to argument (f) Hayashi teaches second secondary IC die (component chip 3) links by second conductive paths to the second surface of the base IC die as described in response (a), (b), (d), and (e).

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 21-24 and 29-30 are rejected under 35 U.S.C. 102(b) as being anticipated by Hayashi et al. (U. S. Patent 5,569,952).

As to claim 21, Hayashi discloses a multiple die electronic system (28-figure 8) as shown in figures 1-16 comprising:

a substrate (5-figure 3, column 5, line 29) having conductors (not shown, column 5, line 30) formed thereon,

a base (2, column 4, line 43) IC die having a first surface facing the substrate and a second surface parallel to the first surface (see figure 3),

a first secondary IC die (3, column 4, line 46) residing between the first surface of the base IC and the substrate and linked to the first surface of the base IC die through first conductive signal paths (2a, column 4, line 49), and

conductive contacts (4, column 4, line 49) extending between the first surface of the base IC die and the conductors on the substrate for conveying signals between the base IC die and the conductors on the substrate.

As to claim 22, Hayashi discloses a multiple die electronic system as shown in figures 1-16 wherein solder (column 4, line 49) forms the first conductive signal paths.

As to claims 23-24, Hayashi discloses a multiple die electronic system as shown in figure 3 wherein the substrate (5) is a printed circuit board substrate or a semiconductor substrate.

As to claim 29, Hayashi discloses a multiple die electronic system as shown in figures 1-16 further comprising:

a second secondary IC die (3-figure 3); and

second conductive paths linking the second secondary IC die to the second surface of the base IC die.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 25-28 and 30-31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hayashi et al. (U. S. Patent 5,969,952) in view of Khandros et al. (U. S. Patent 6,330,164).

As to claims 25-28, and 31, Hayashi discloses a multiple die electronic system as shown in figures 1-16 wherein the conductive contacts (4) are formed on the first surface of the base IC die (2) and soldered to the conductors on the substrate (5-figure 3). Hayashi does not teach the conductive contacts are resilient spring contacts.

Khandros shows conductive resilient spring contacts (21-figure 2) connected between IC base (12) and a substrate (10).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to use resilient spring contacts as taught by Khandros to employ the multiple die electronic system in order to provide a high volume, low cost manufacturing process, and geometry protuberant conductive contacts.

As to claim 30, Khandros shows an interconnection assembly as shown in figures 2 and 4B comprising conductive vias (23, or 23A) for providing signal paths between the first and second surfaces of the base IC die.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to utilize conductor vias as taught by Khandros to employ the system of Hayashi in order to provide an electrical connection between two surface of a substrate or a PCB.

As to claim 31, Hayashi discloses a multiple die electronic system as shown in figures 1-5 wherein the second conductive paths comprise spring contacts.

Conclusion

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tuan T Dinh whose telephone number is 703-306-5856. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David L. Talbott can be reached on 703-305-9883. The fax phone numbers for the organization where this application or proceeding is assigned are 703-305-1341 for regular communications and 703-305-1341 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

Albert W. Paladini 11-18-02

ALBERT W. PALADINI
PRIMARY EXAMINER

TD
November 15, 2002.